

FIG. 1

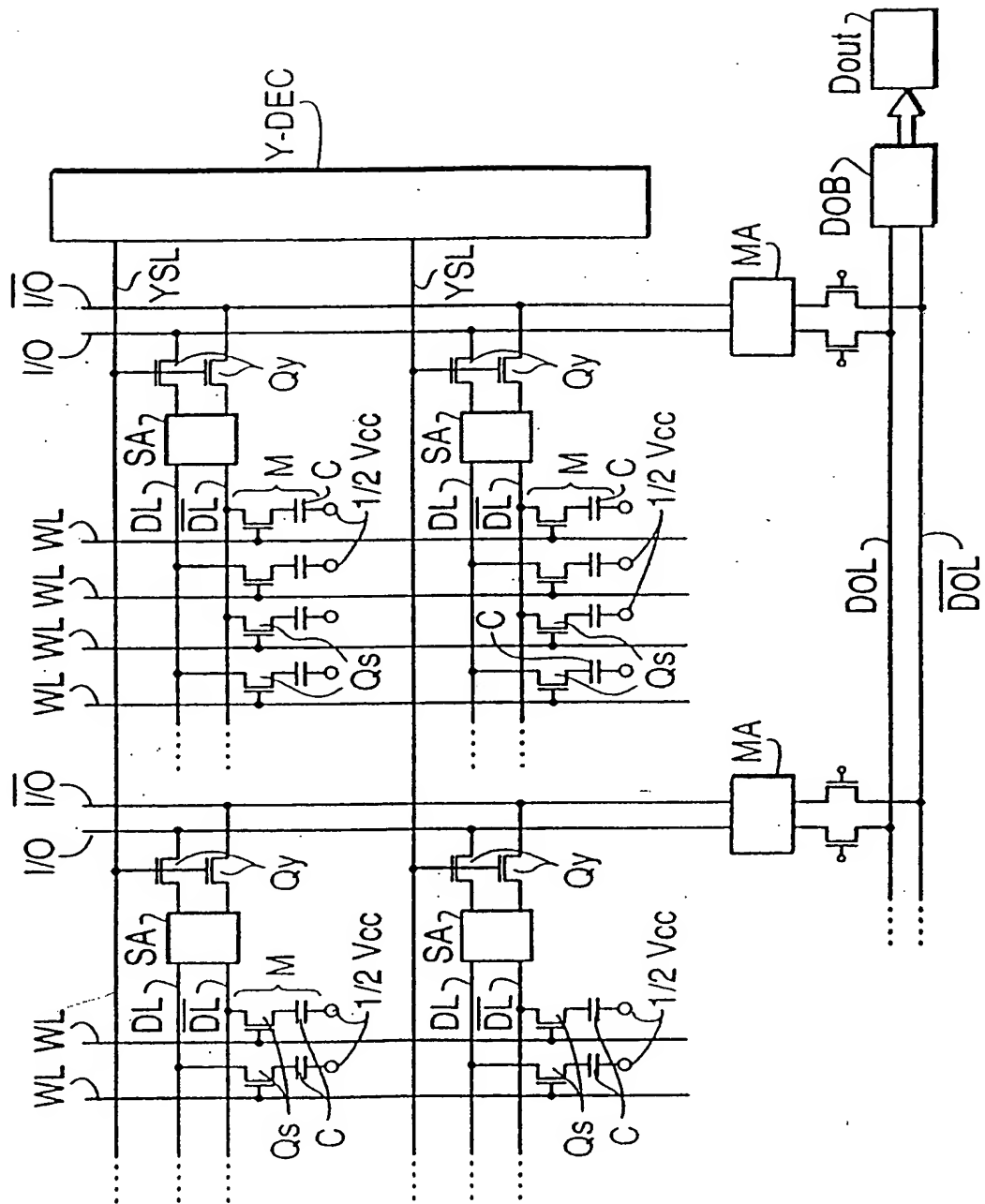
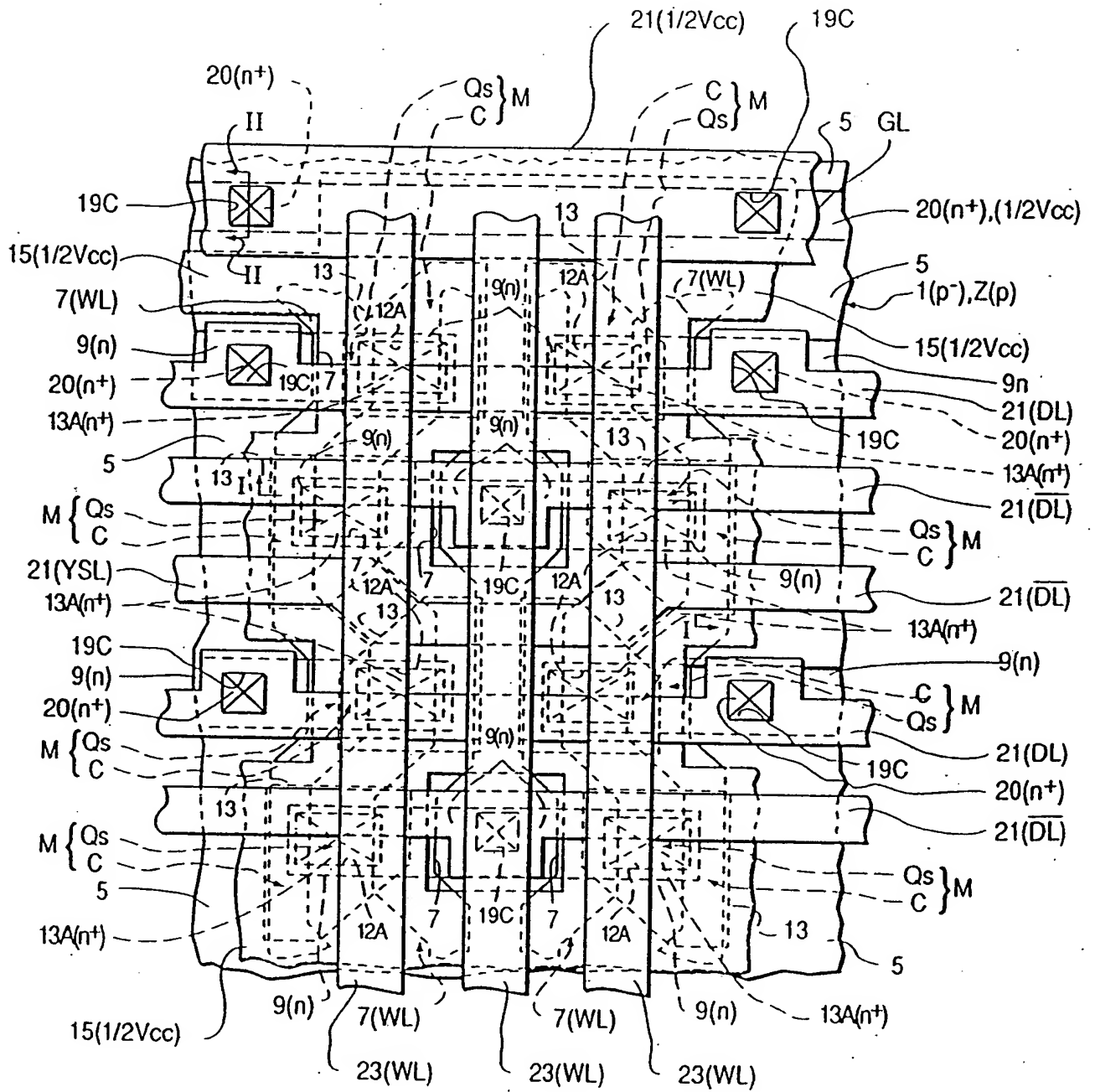


FIG. 2



[illegible]

FIG. 4

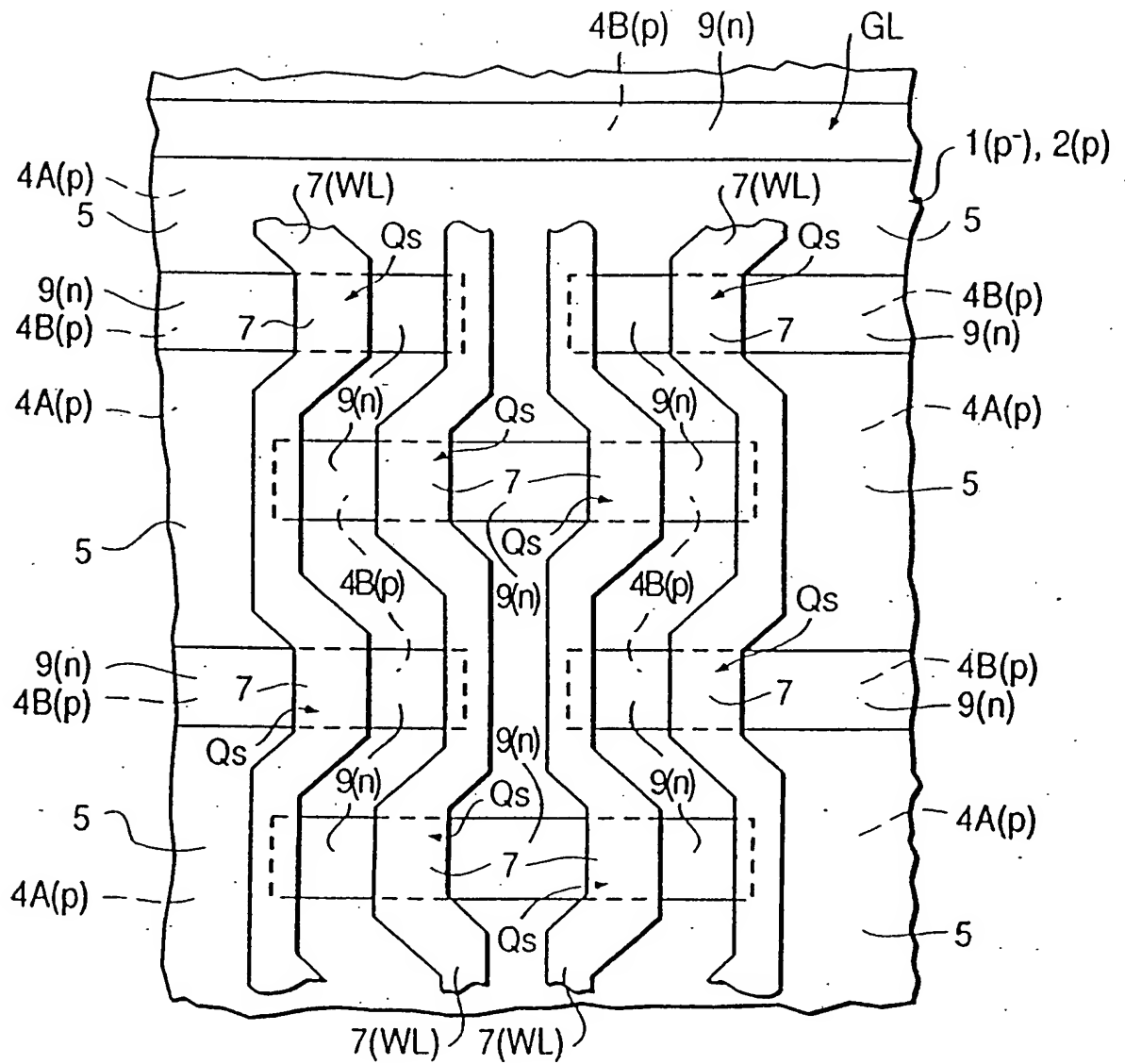


FIG. 5

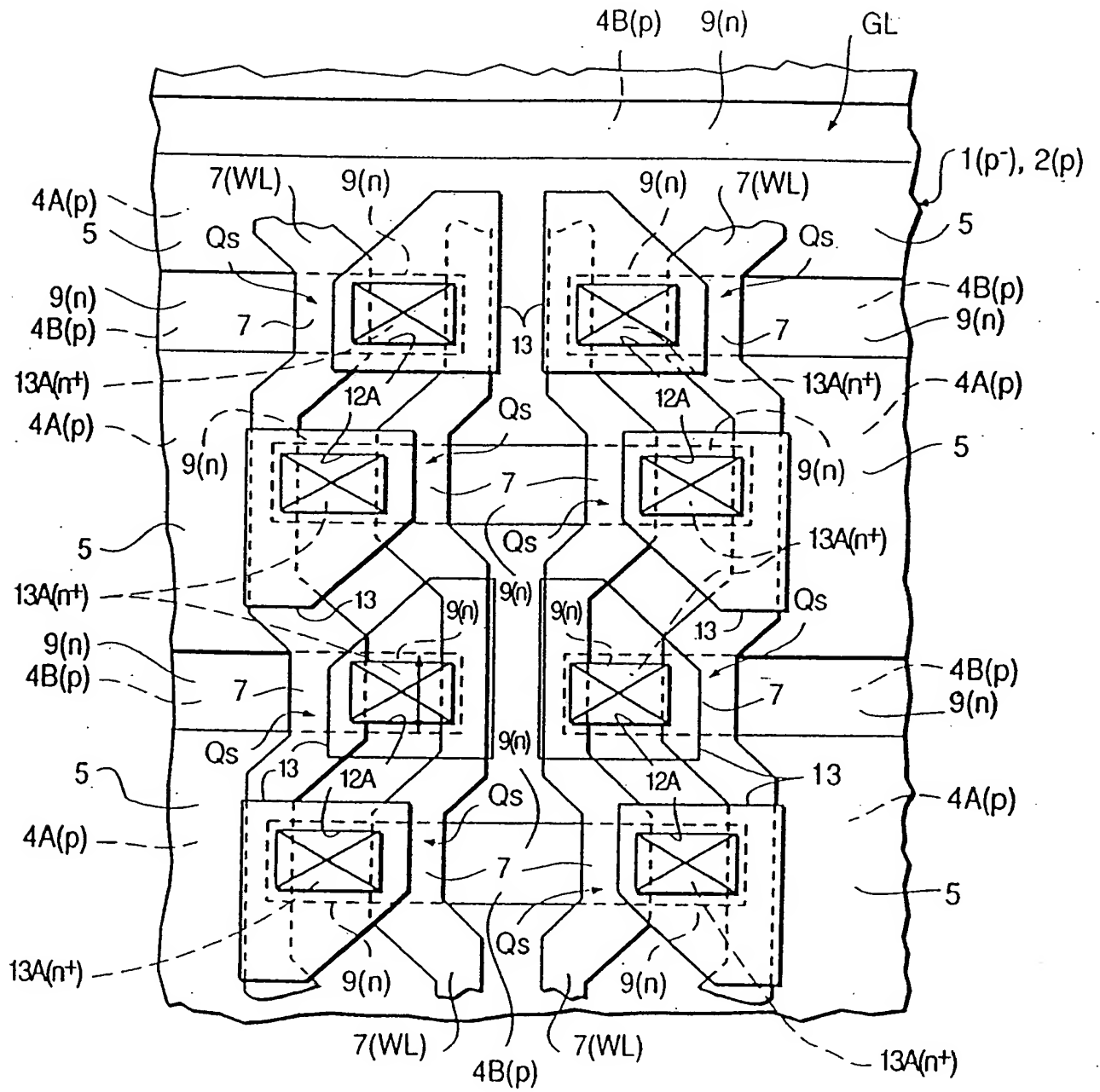


FIG. 6

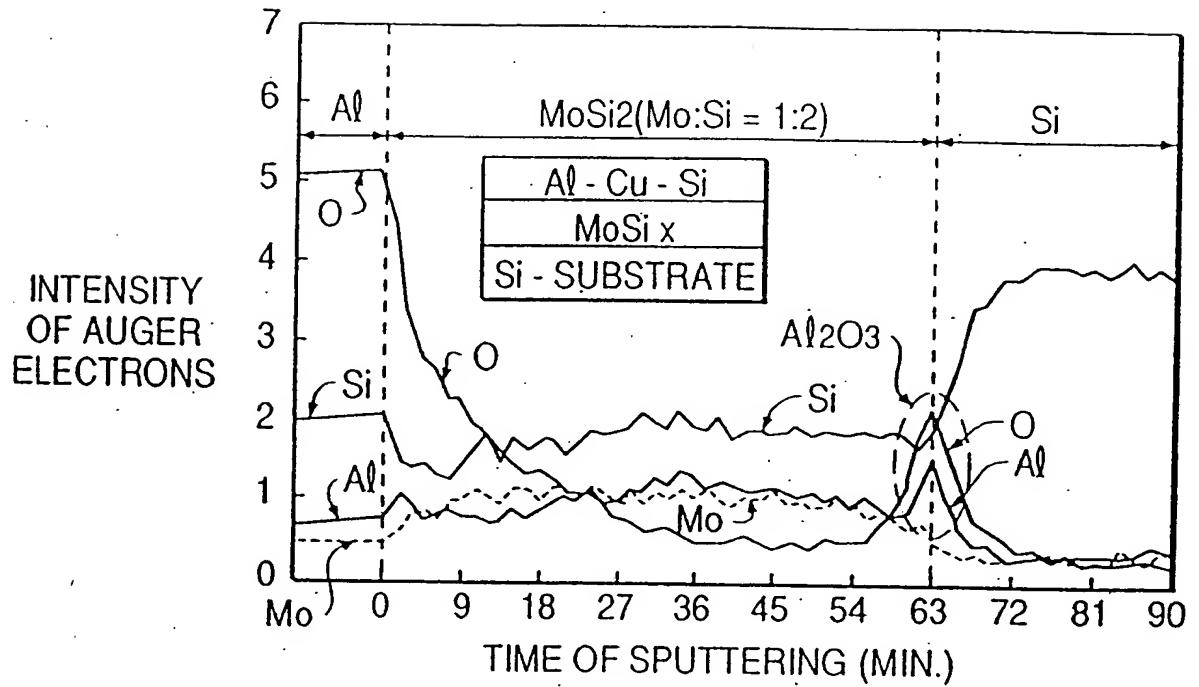


FIG. 7

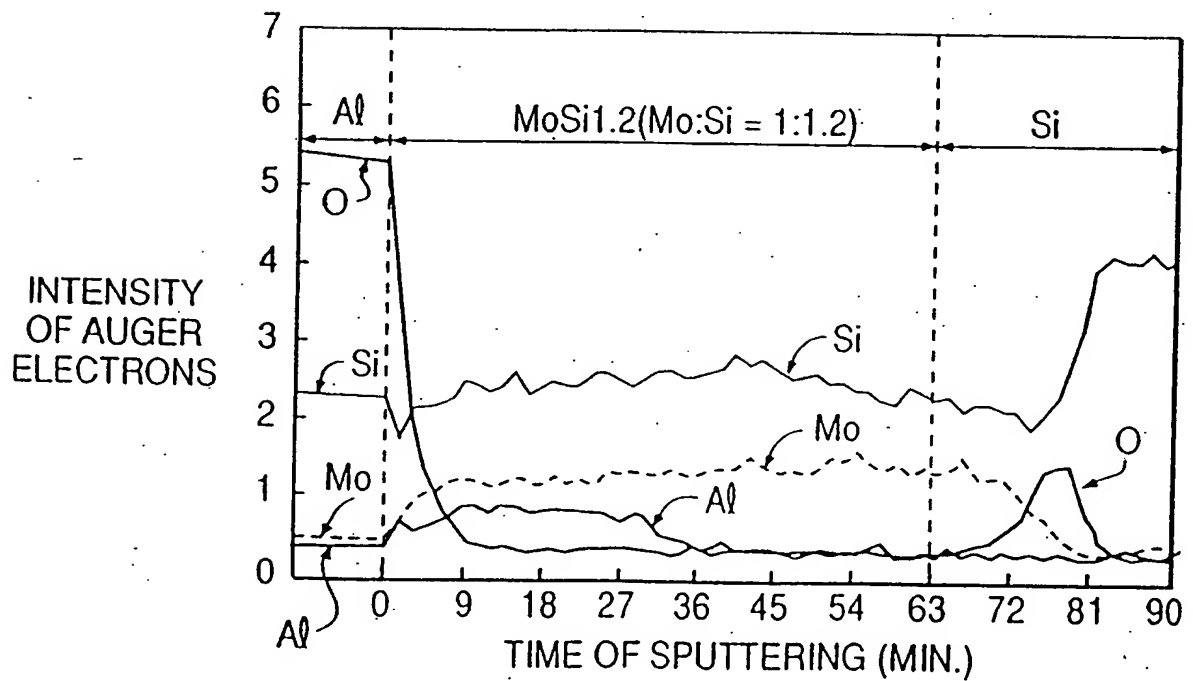


FIG. 8

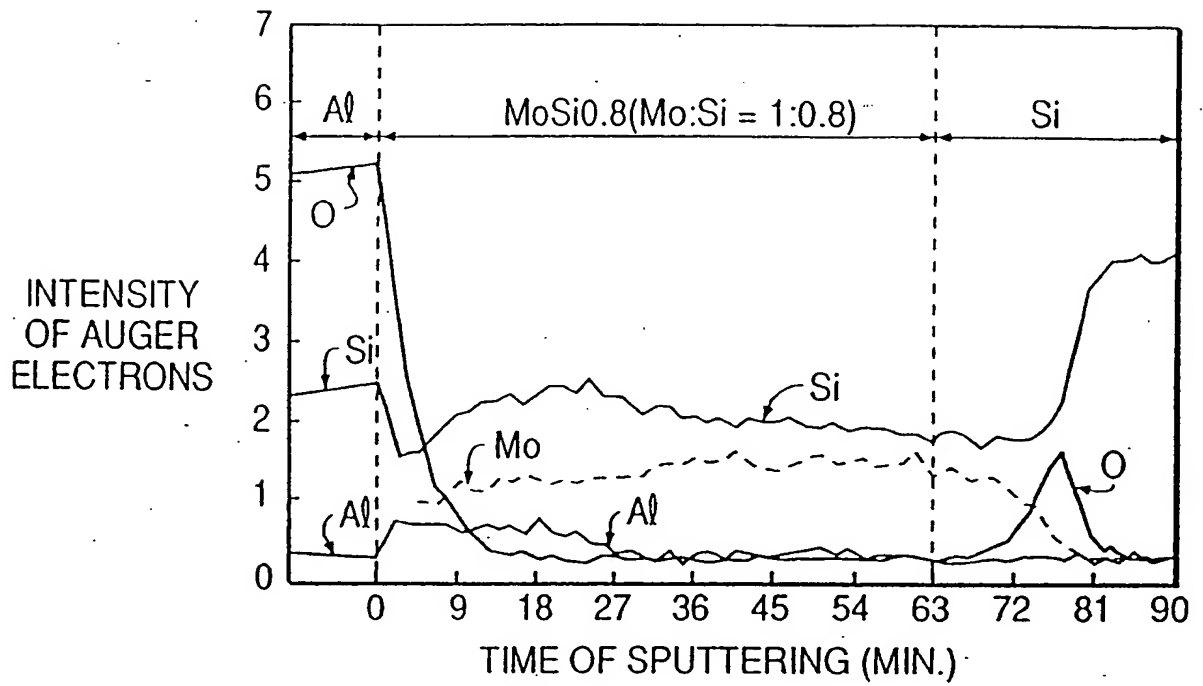


FIG. 27

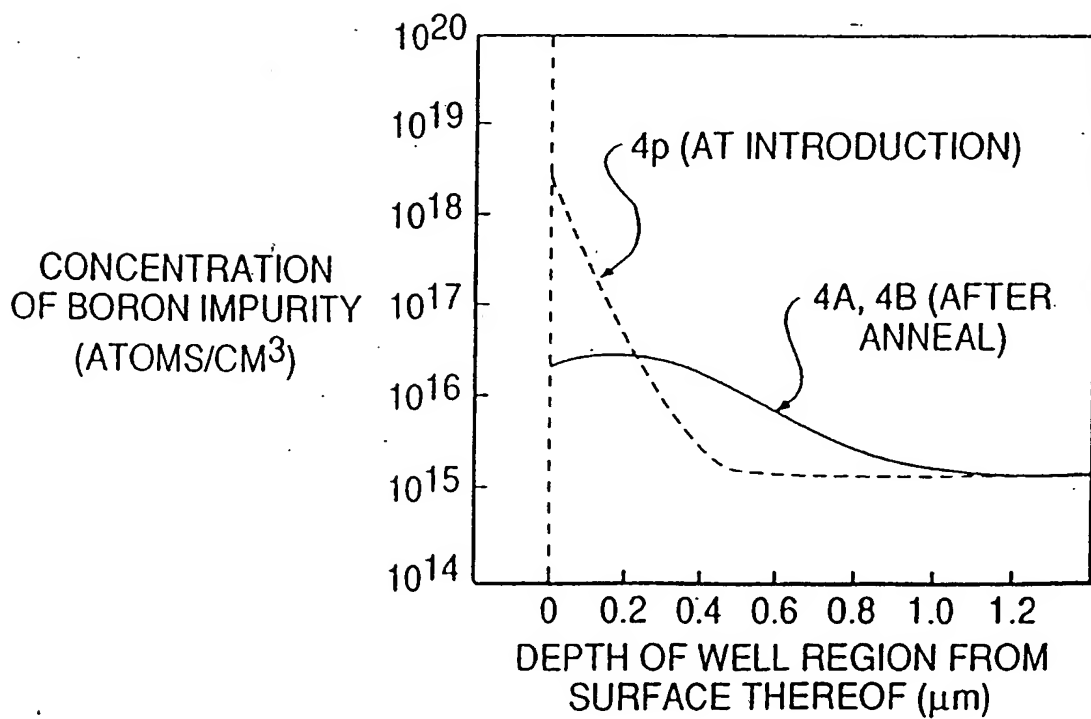


FIG. 9

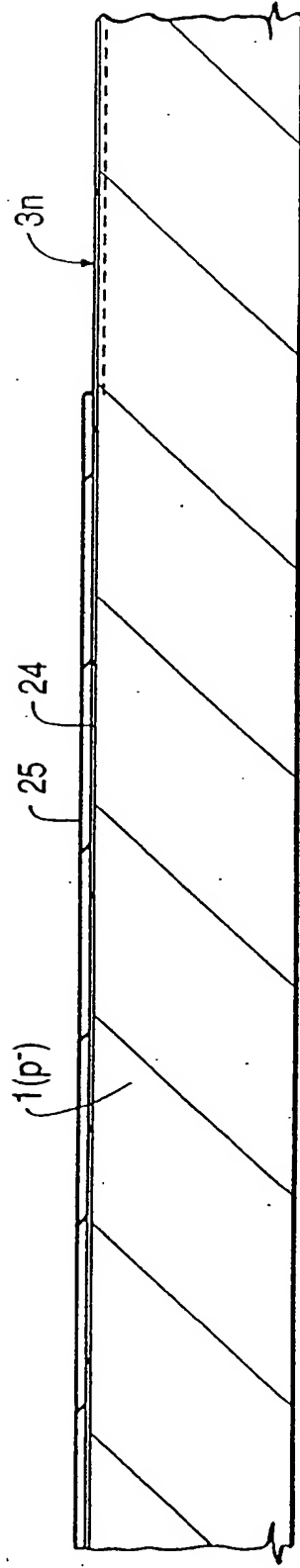


FIG. 10

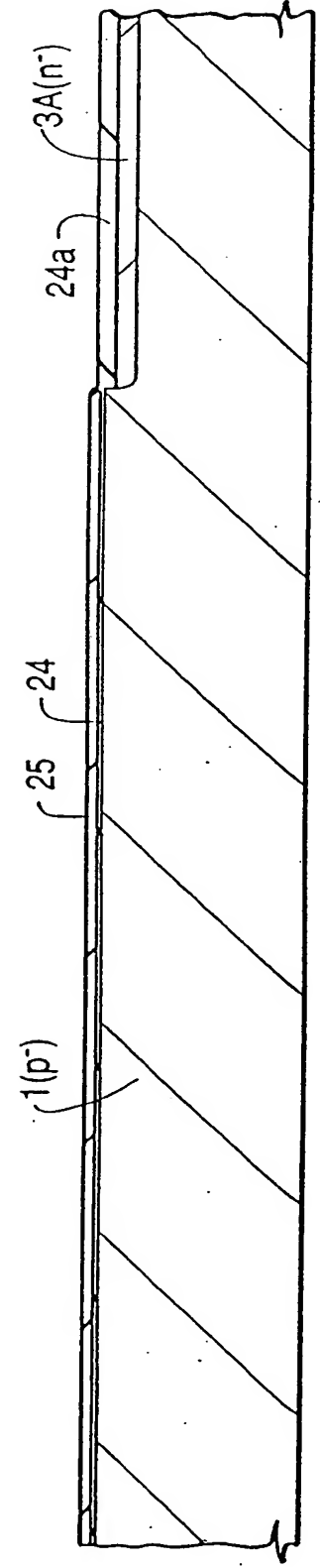


FIG. 11

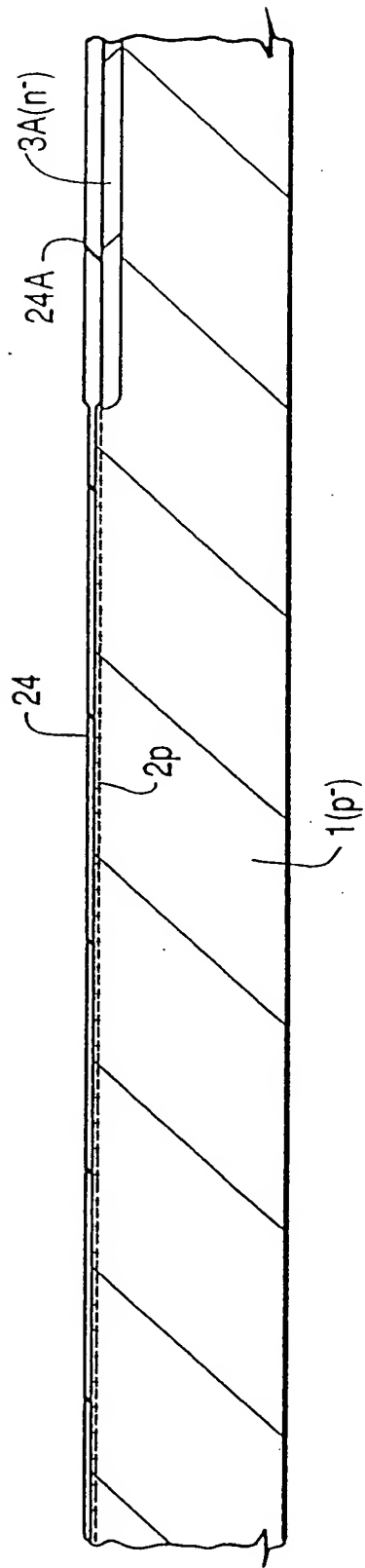


FIG. 12

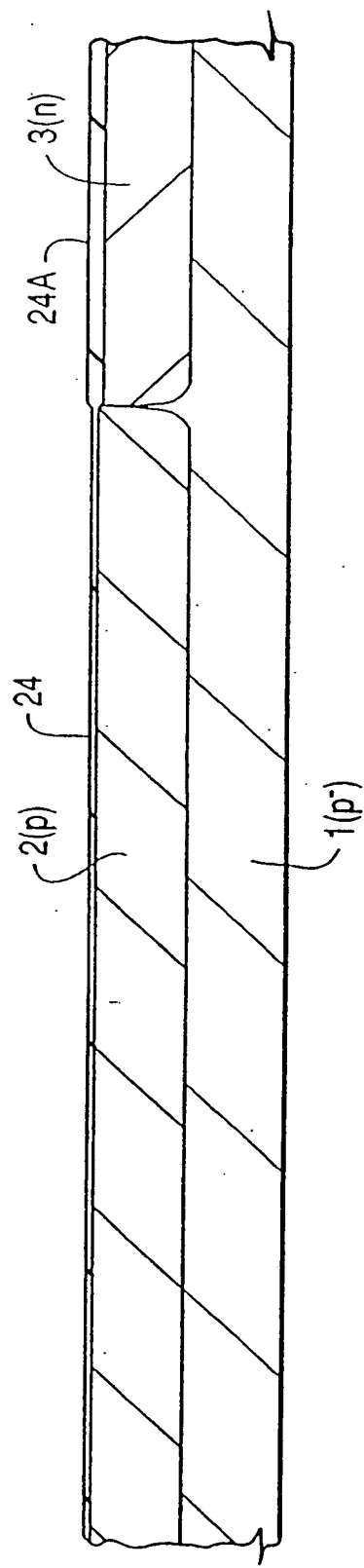


FIG. 13

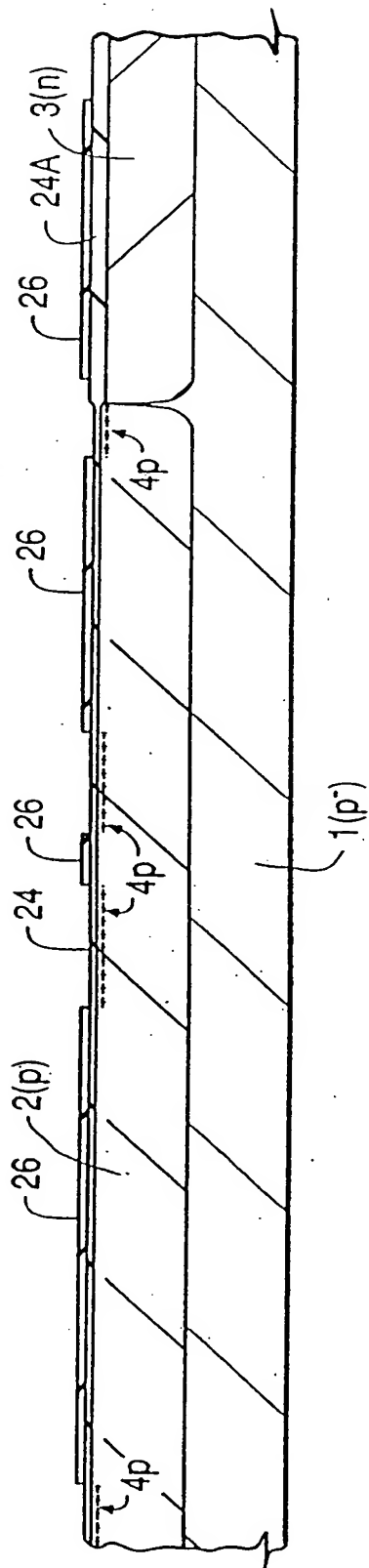


FIG. 14

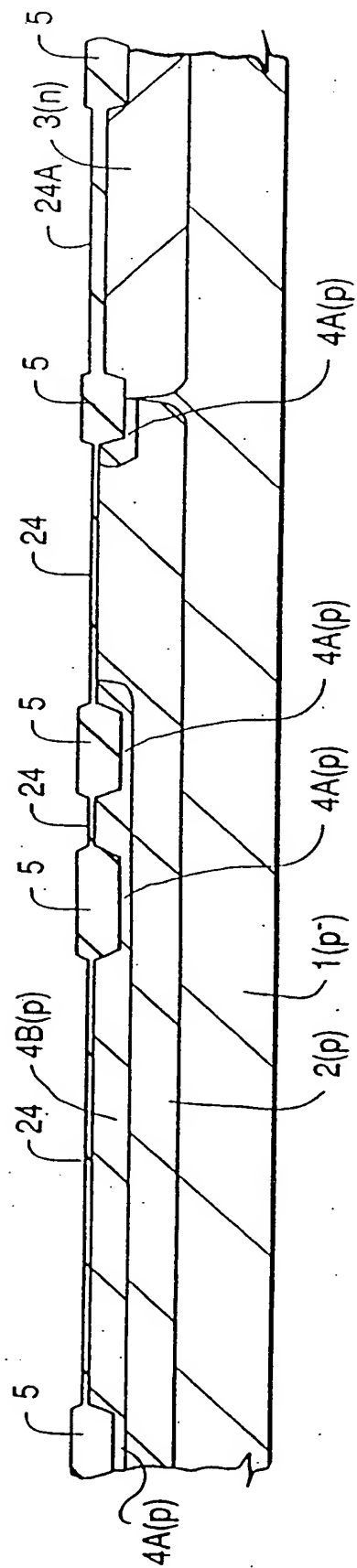


FIG. 15

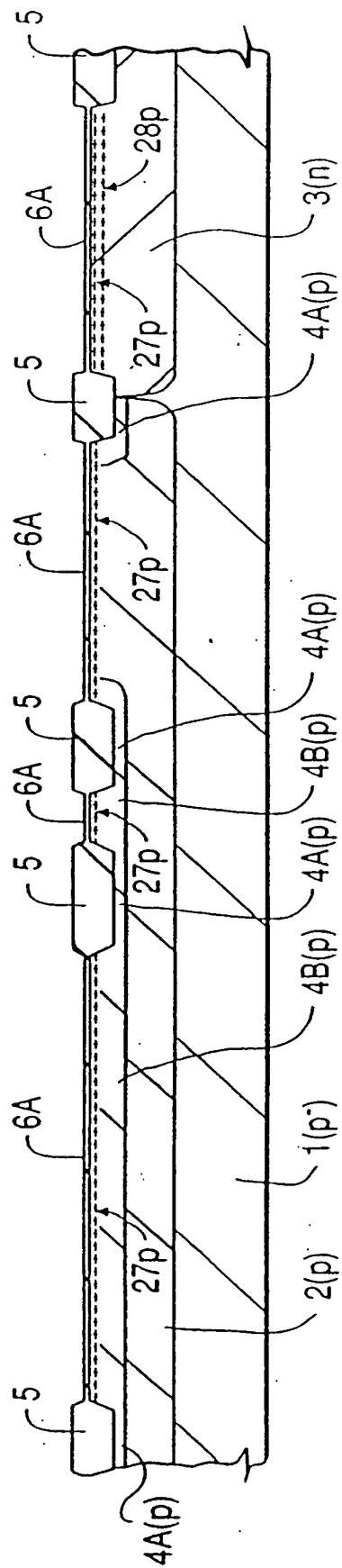


FIG. 16

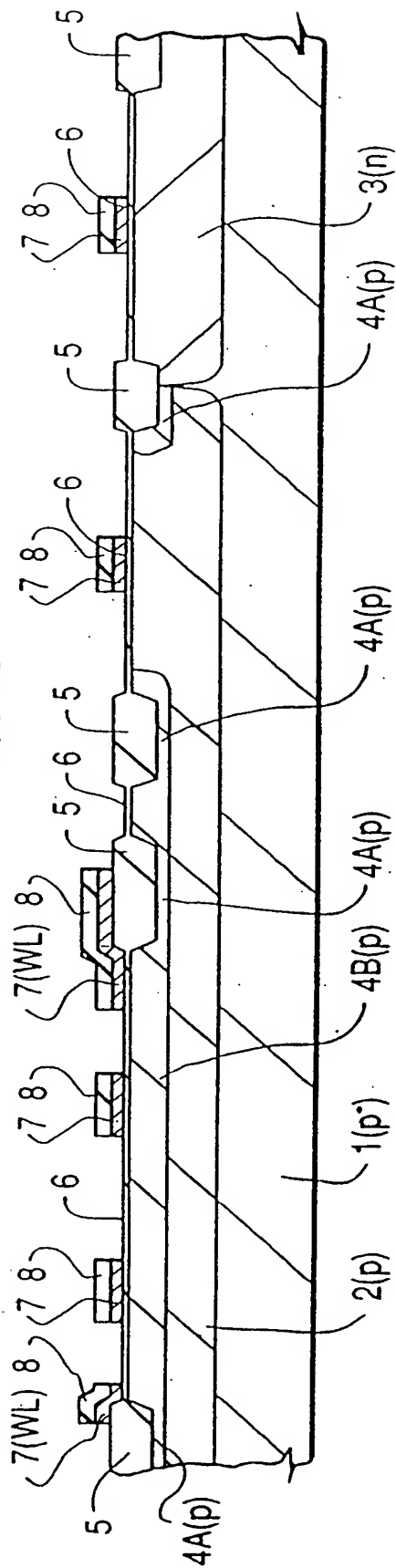


FIG. 17

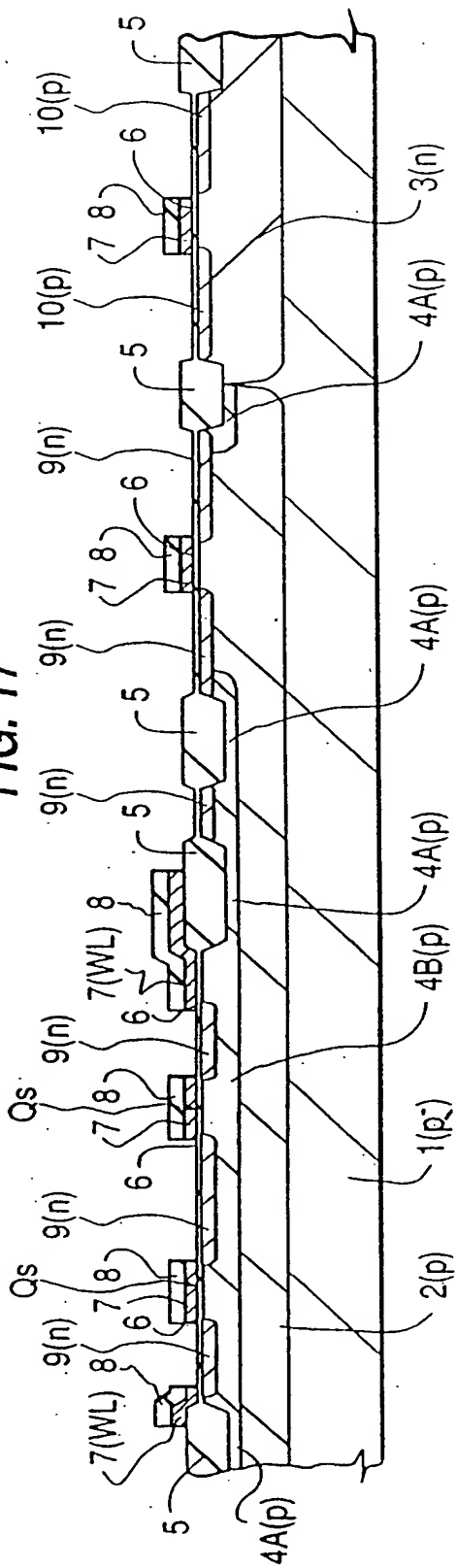


FIG. 18

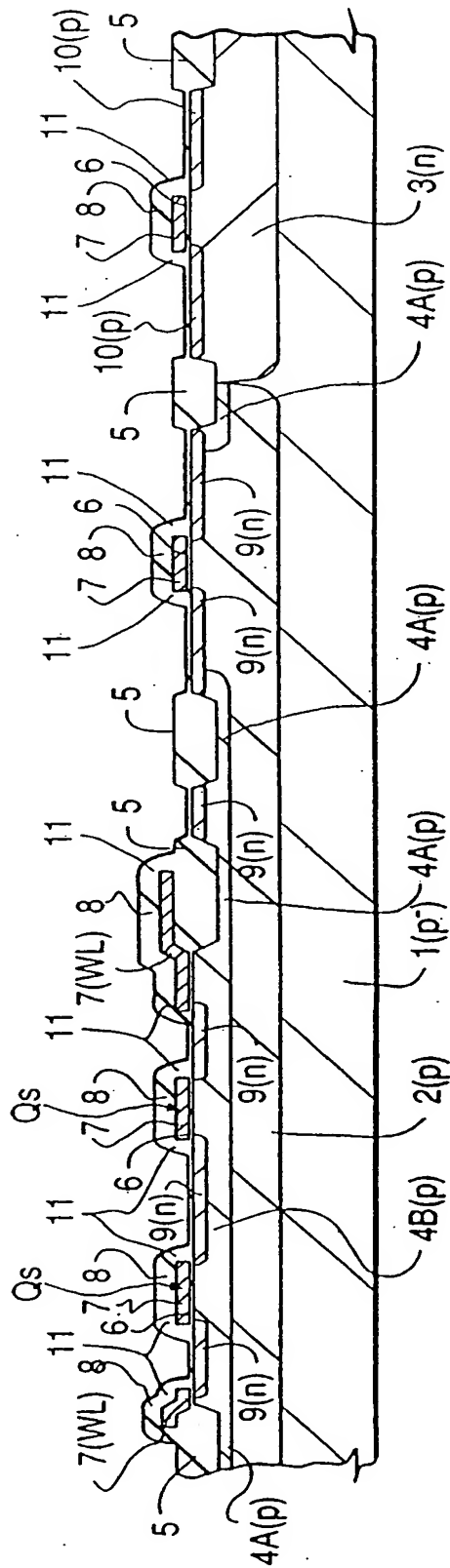


FIG. 19

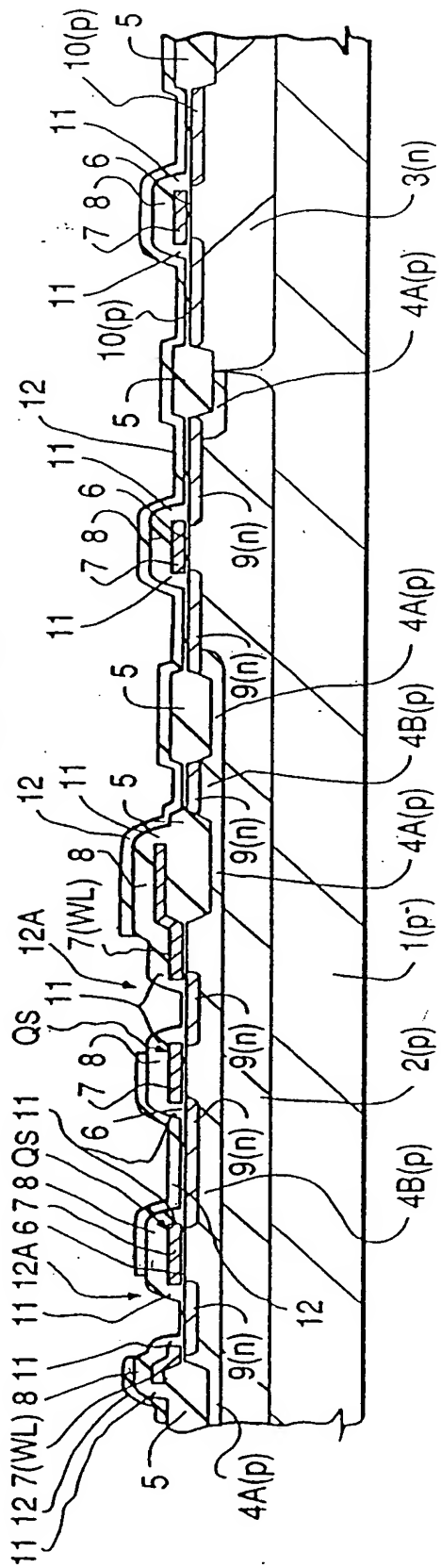


FIG. 20

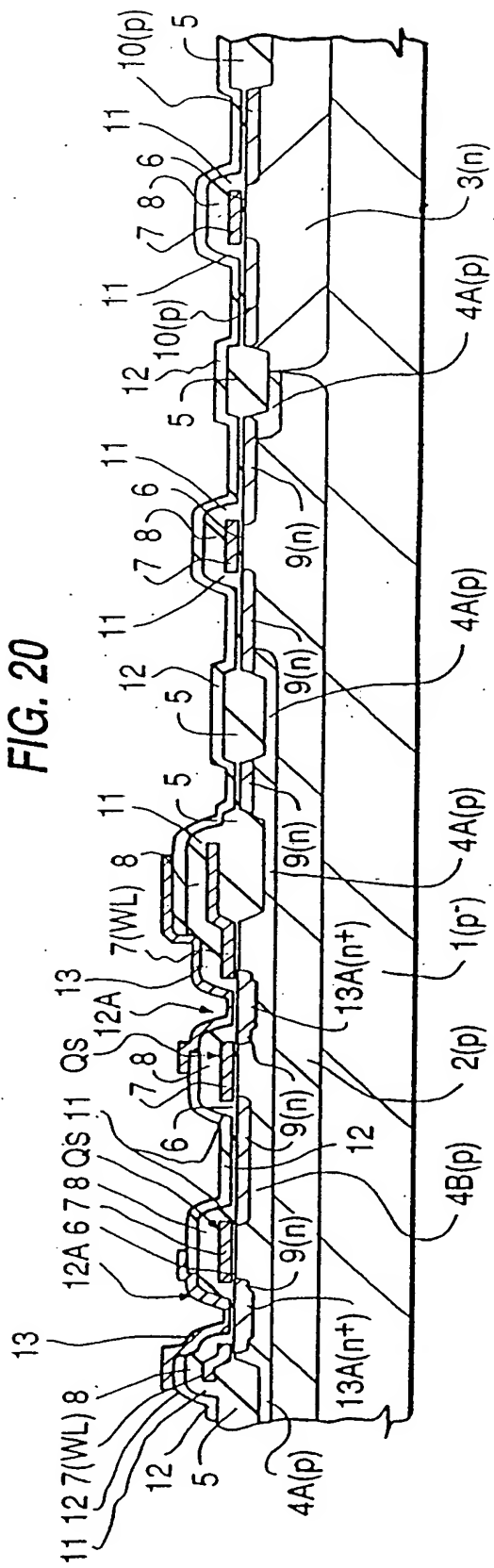


FIG. 21

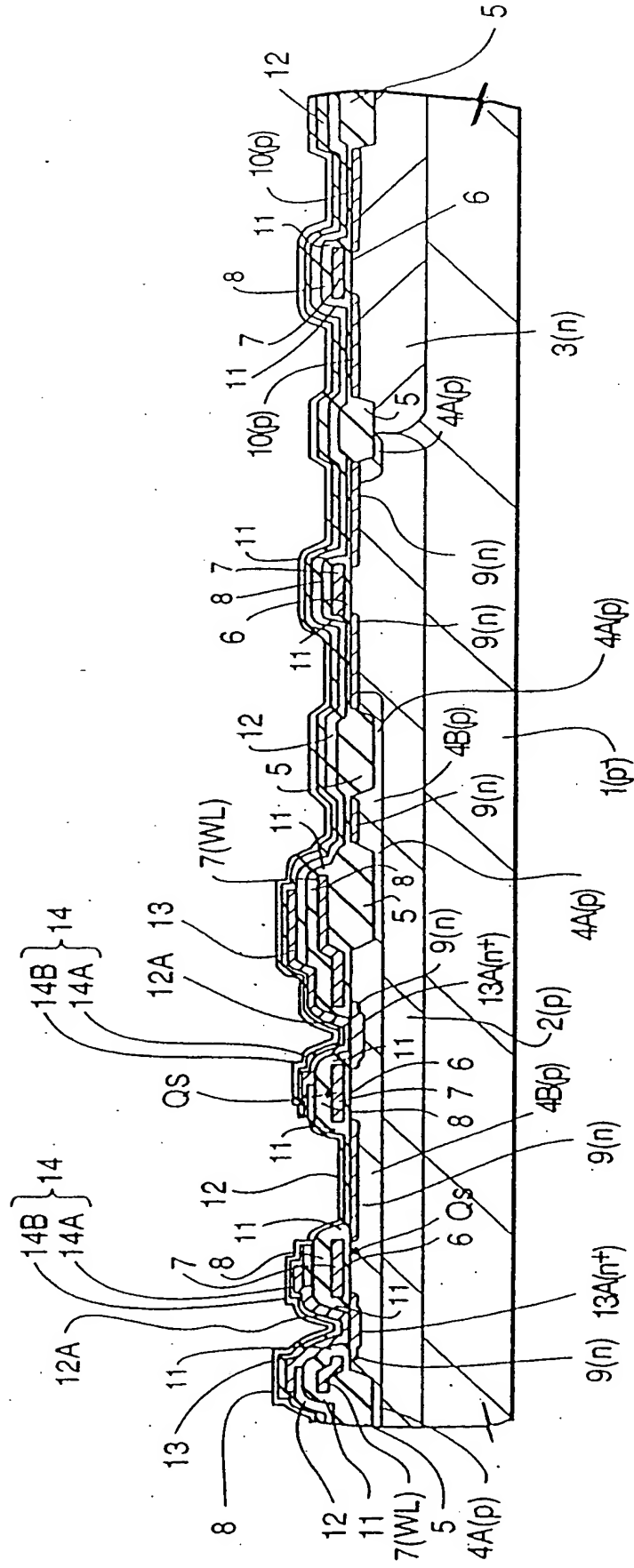


FIG. 22

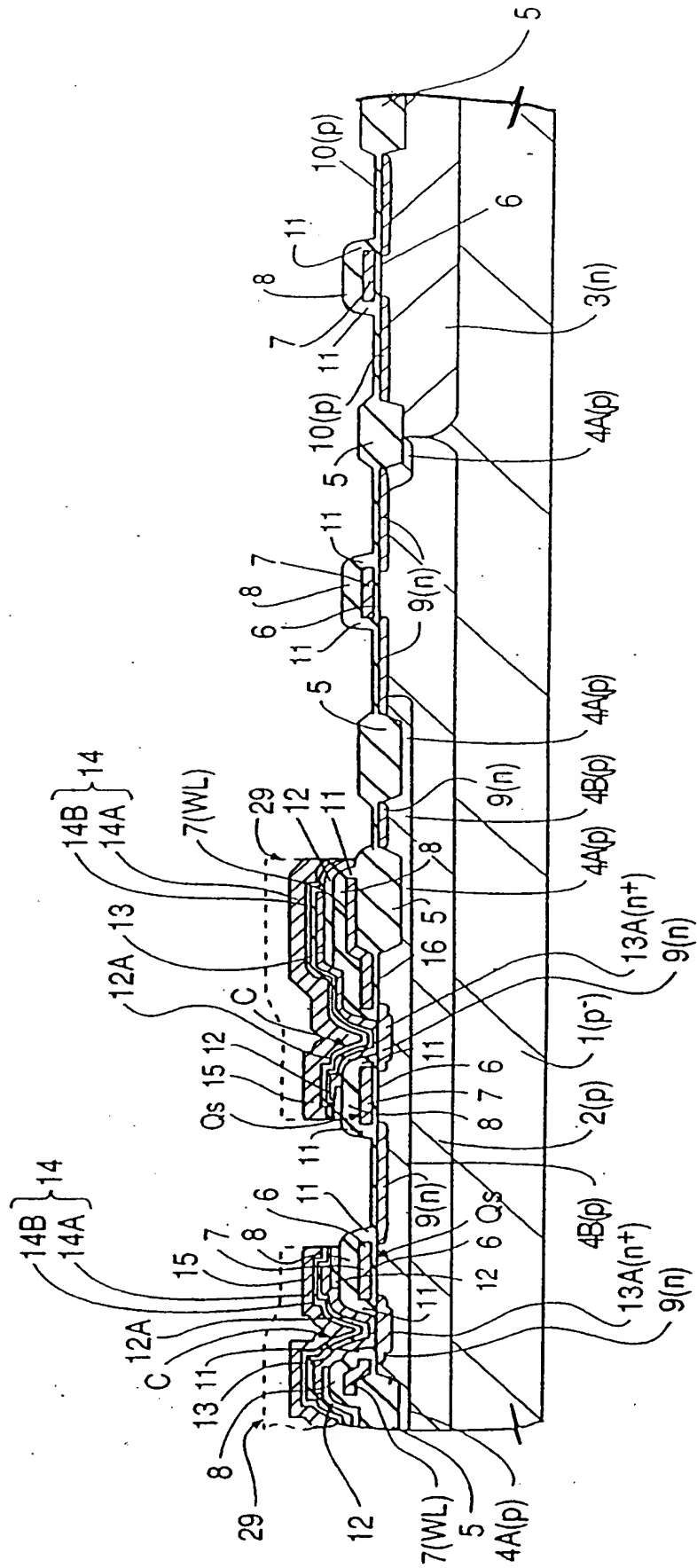
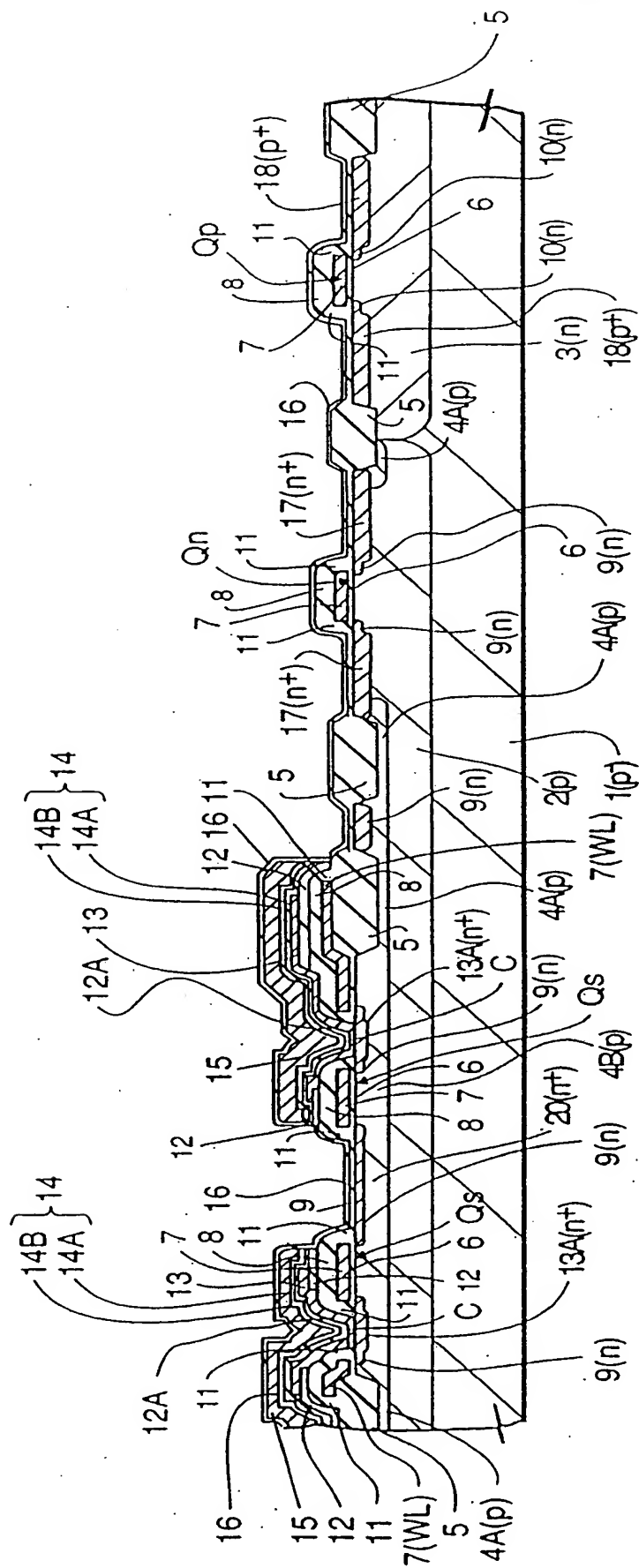


FIG. 23



The diagram shows a cross-section of a semiconductor device with multiple memory cells. The structure includes a substrate (1) with a p-type region (1(p)). A series of word lines (WL) and bit lines (BL) are shown crossing over each other. The device features access transistors (Qs) and storage capacitors (Cs). Various conductive layers (5, 6, 7, 8, 9(n), 10(p), 11, 12, 13, 14A, 14B, 15, 16) and dielectric layers (17, 18, 19A, 19B, 19C) are present. Contact regions (20(n+), 20(p)) are also indicated. A central region is labeled 'C' and 'C''.

FIG. 26

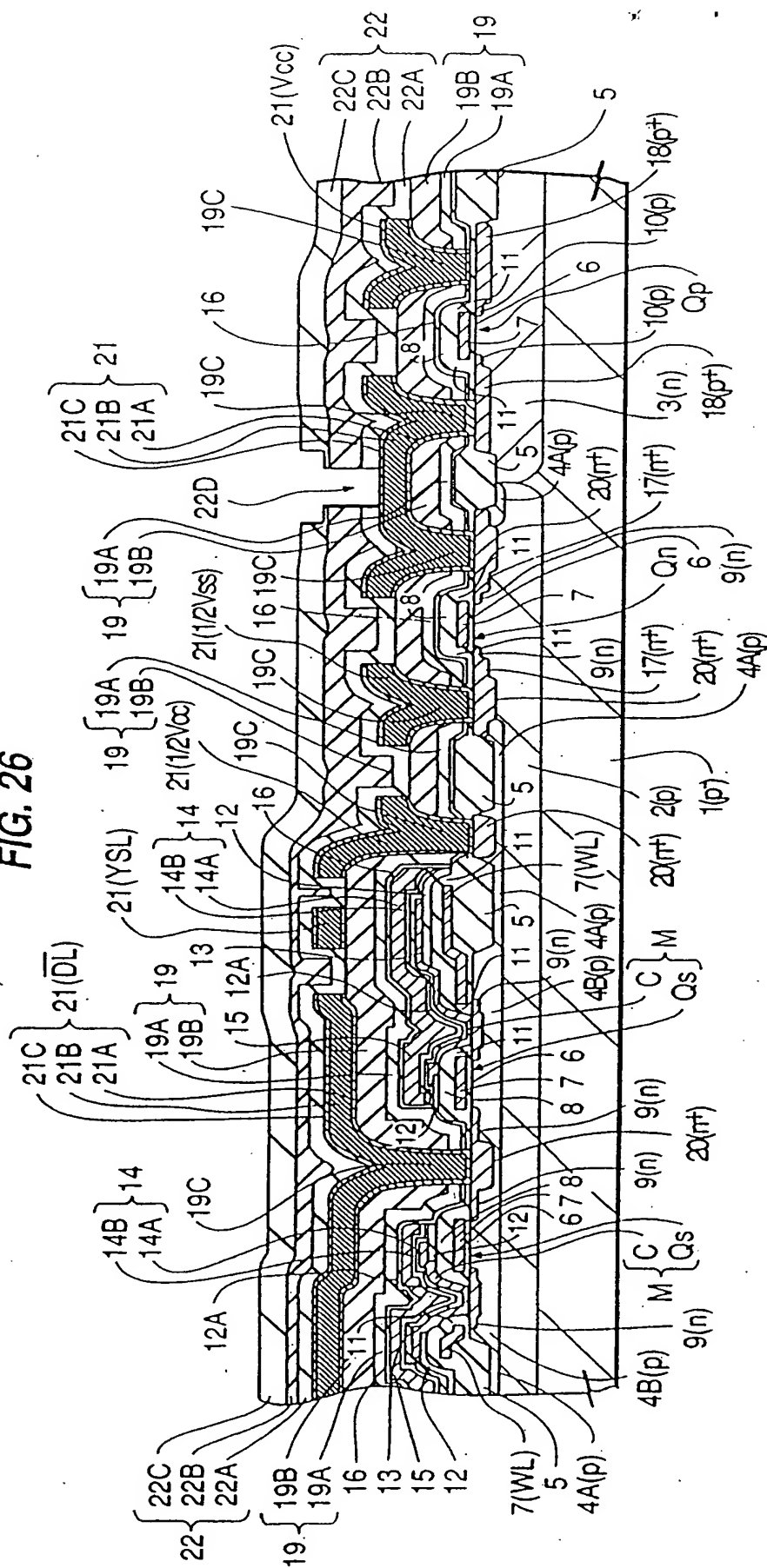


FIG. 28

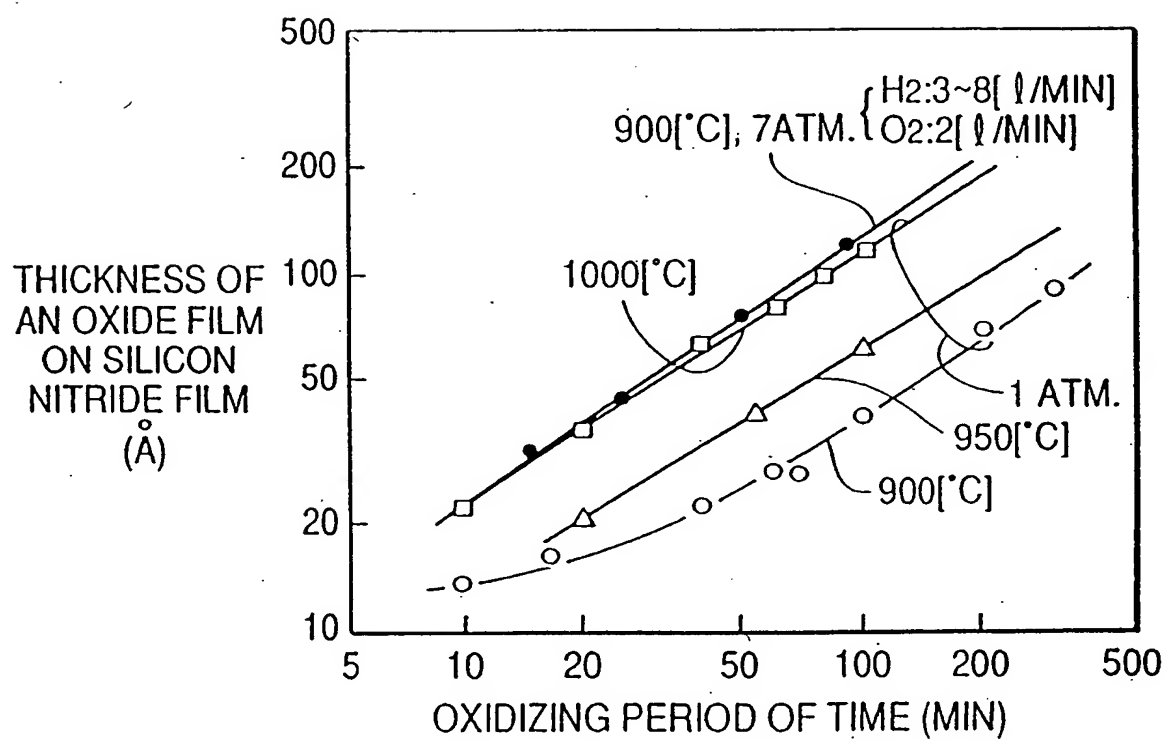


FIG. 29

